(19) Japan Patent Office (JP)

(12) **KOKAI TOKKYO KOHO** (A)
[OFFICIAL GAZETTE FOR UNEXAMINED PATENT APPLICATIONS]

(11) Japanese Patent Application Kokai Publication Number: **H09-252117**

(43) Publication Date: September 22, Heisei 9 (1997)

(51) Int. Cl.[6]	I.D.Code	JPO File No.	FI		
H 01 L 29/78			H 01 L 29/78	301G	
21/265			21/265	V	

Examination Requested: Not yet requested
Number of Claims: 4 OL (7 pages in total) [Japanese text]

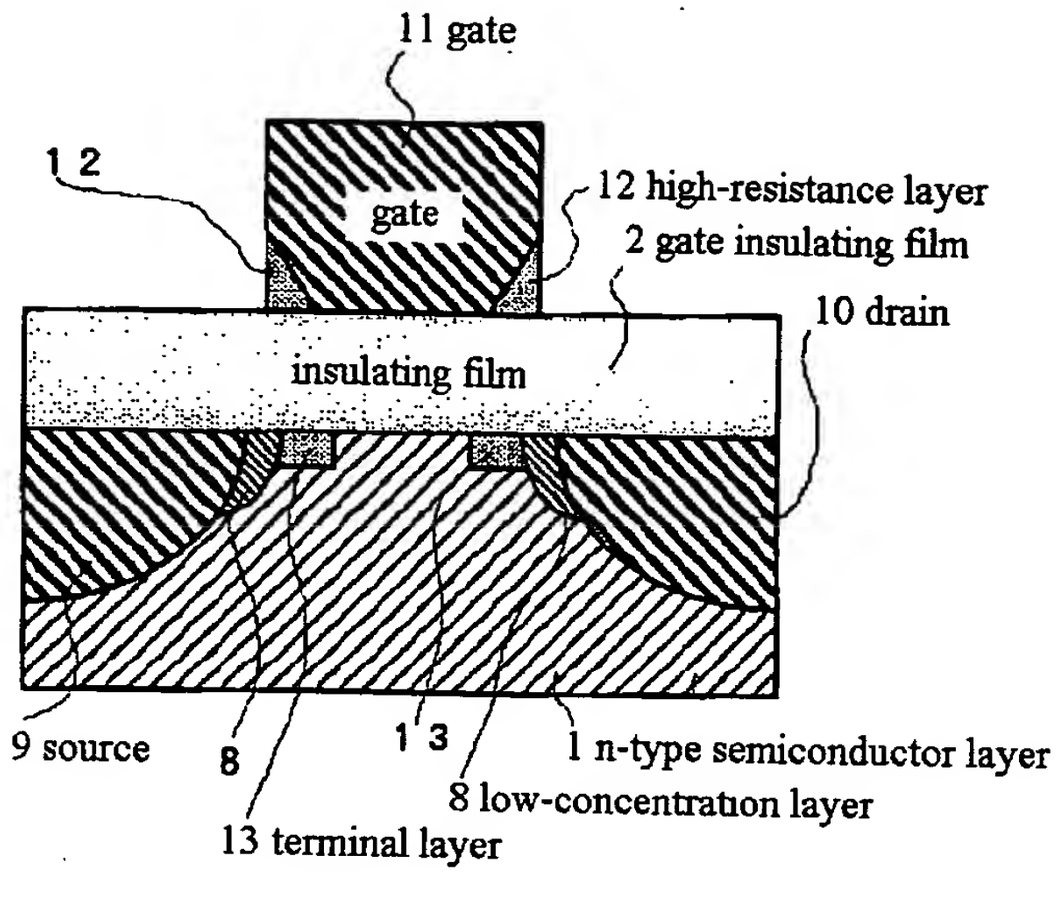
(21) Application Number: H08-57710
(22) Application Date: March 14, Heisei 8 (1996)
(71) Applicant: 000001889
Sanyo Electric Co. Ltd. [Sanyo Denki Kabushiki Kaisha]
5-5, Keihan Hondori 2-chome, Moriguchi, Osaka Prefecture, Japan
(72) Inventor: Sasada Kazuhiro
C/O Sanyo Electric Co. Ltd.
5-5, Keihan Hondori 2-chome, Moriguchi, Osaka Prefecture, Japan
(74) Agent: Okada Kei, patent attorney

(54) **TITLE OF THE INVENTION:** Field-effect transistor

(57) **ABSTRACT**

PROBLEM TO BE SOLVED: To suppress fluctuations in the threshold voltage caused by the phenomenon of BF_2 (difluoroborane) penetration into the p-channel and an increase in the current leakage due to the generation of near-interface states in the gate or the gate insulating film caused by boron (B), when ions are implanted into a p-channel field-effect transistor,

SOLUTION: Fluorine (F) ions are implanted obliquely into a gate 11 using the accelerated voltage of 10 to 100 keV and a dose of 1×10^{11} to 1×10^{16} cm^{-2}, to form, under a gate insulating film 2, a low-concentration layer 8 having a B concentration of 2×10^{12} to 2×10^{16} cm^{-3} and a terminal layer 13 having an F concentration of 2×10^{12} to 2×10^{16} cm^{-3}. As well, a high-resistance layer 12 is formed at the lower sides of the gate 11. In this manner, the degradation of the insulation at both edges of the gate is prevented by lowering the effective voltage and increasing the distance, and the near-interface states, which can cause current leakage, are eliminated by the strong bond energy of F.


11 gate
12
gate
12 high-resistance layer
2 gate insulating film
10 drain
insulating film
9 source
8
13
8
13 terminal layer
8 low-concentration layer
1 n-type semiconductor layer

CLAIMS

What is claimed is:

1. A field-effect transistor, wherein the concentration of the dopant is high in the section at the lower sides of the gate.

2. A field-effect transistor according to claim 2, wherein the dopant in the gate is halogen.

3. A method of manufacturing a field-effect transistor, comprising:

a step for forming a gate insulating film on a semiconductor layer;

a step for forming an island-form polycrystalline layer on the gate insulating film;

a step for forming an impurity layer on the surface of the semiconductor layer and on the island-form polycrystalline layer by implanting impurity ions into these layers;

a step for forming a high-resistance layer and a terminal layer by implanting fluorine ions obliquely into the lower sides of the island-form polycrystalline layer and into the semiconductor layer, respectively; and

a step for implanting impurity ions into the impurity layer on surface of the island-form polycrystalline layer on the gate insulating film and into the impurity layer on the surface of the semiconductor layer.

4. A method of manufacturing a field-effect transistor, comprising:

a step for forming a gate insulating film on a semiconductor layer;

a step for forming an island-form polycrystalline layer on the gate insulating film;

a step for forming an impurity layer on the surface of the semiconductor by implanting impurity ions into the semiconductor layer; and

a step for forming a high-resistance layer and a terminal layer by implanting fluorine ions obliquely into the lower sides of the island-form polycrystalline layer and into the semiconductor layer, respectively.

DETAILED DESCRIPTION OF THE INVENTION

[0001]
Technical Field of the Invention: The present invention relates to the constitution of a field-effect transistor and a method of manufacturing the same.

[0002]
Description of Related Art: A method of manufacturing a field-effect transistor having a lightly doped drain (LDD) structure, such as the one referred to in Kokai Publication No. S58-142566, for example, will be described with reference to the accompanying Fig. 6. As seen in Fig. 6a, a gate insulating film 2 is formed on an n-type semiconductor layer consisting of mono-crystalline silicon, and an island-form polycrystalline layer 3 composed of polycrystalline silicon is formed over it.

[0003] Next, boron (B) ions, which have been accelerated in a reduced-pressure environment, are implanted vertically into the n-type semiconductor layer 1. This results in the formation of a p^+ layer 4 on the surface of the island-form polycrystalline layer 3 and [under the gate insulating film] on both sides of the island-form polycrystalline layer 3, as shown in Fig. 6b. The entire island-form polycrystalline layer formed on the gate insulating film 2 is then turned into a p layer 5 by heat treatment, whereas the p^+ layer under the gate insulating film 2 is turned into a thick p layer 6 to act subsequently as the low-concentration layer of an LDD, as shown in Fig. 6c.

[0004] As shown in Fig. 6d, insulative sidewalls 7 are formed by depositing oxidized silicon all at once on the entire surface by thermal chemical vapor deposition (CVD) and then by etching carried out in a manner so as to leave intact the oxidized silicon on the sides of the p layer 5 lying on the gate insulating film. As shown in Fig. 6e, BF_2 ions, which have been accelerated under reduced pressure, are implanted vertically into the n-type semiconductor layer 1.

[0005] Here, the sidewalls 7 formed prior to this serve as the film to prevent the impurity BF_2 from becoming implanted. Consequently, because the B concentration of the sections of the p layer lying under the sidewalls 7 is not raised, they become low-concentration layers 8, as shown in Fig. 6f. At the same time, a source 9 and a drain 10 are formed under the gate insulating film 2 in the area adjacent to the sidewalls 7.

[0006] Moreover, because the B concentration of the p layer on the gate insulating film 2 is raised as a result of the BF_2-ion implantation, its resistance becomes low and is turned into a polycrystalline gate 11. P-type polycrystalline silicone is manufactured in this manner by implanting BF_2 or B ions into polycrystalline silicon, followed by heat treatment to activate it.

[0007]
Problems to be Solved by the Invention: However, side effects produced by the ion implantation vary depending upon the ion species used. For instance, BF_2 has a disadvantage in

that the use of this ion species causes B contained in the gate to pass through the gate oxide film and to reach the channel surface, thereby altering the threshold value Vt of the transistor.

[0008] On the other hand, the use of B ion species, although it does not cause the penetration to the channel surface as is the case with BF_2, poses a problem of increased near-interface states in the Si-SiO_2 boundary. It is thought that F, which constitutes the fragment of the decomposition of BF_2, is largely responsible for whether B passes from the gate, through the gate insulating film, to reach the channel surface (J.M. Sung et al., "Fluorine Effect Boron Diffusion of P^+ Gate Devices", *IEDM* (1989) pp447–450.).

[0009] According to the above article, when B, which is initially present in the gate, passes from there, through the gate insulating film, to reach the channel, it tends to form B_2O_3 in the oxide film. The explanation offered in the article speculates that, if F is also present, then the formation of B_2O_3 is prevented by F, thus allowing for the penetration of B.

[0010] Even though it causes the phenomenon of penetration to the channel surface, F is effective in reducing near-interface states because of its property to terminate dangling bonds present in the Si-SiO_2 boundary. The present invention was developed in consideration of the situation outline above. Therefore, the object of the present invention is to provide a field-effect transistor that is highly resistant to pressure*, and this is achieved by applying electric field of an intensity lower than that found at the center of the gate on the terminal layer, which has few defects, from the two edges of the gate, where the concentration of impurities, which affect conductivity, has been reduced to a relatively low level.

[0011]
Means for Solving the Problems: The field-effect transistor of the present invention is provided with high dopant concentration under the lower sides of the gate. As well, the field-effect transistor of the present invention uses halogen as the dopant to be added to the gate.

[0012] Furthermore, the method of manufacturing a field-effect transistor of the present invention includes: a step for forming a gate insulating film on a semiconductor layer; a step for forming an island-form polycrystalline layer on the gate insulating film; a step for forming impurity layers on the surface of the semiconductor layer and on the island-form polycrystalline layer by implanting impurity ions into these layers; a step for forming a high-resistance layer and a terminal layer by implanting F ions obliquely into the lower sides of the island-form polycrystalline layer and into the semiconductor layer, respectively; and a step for implanting impurity ions into the impurity layer on the island-form polycrystalline layer lying on the gate insulating film and the impurity layer on the surface of the semiconductor layer.

[0013] In another aspect of the present invention, the method of manufacturing the field-effect transistor includes: a step for forming a gate insulating film on a semiconductor layer; a step for

---

* Translator's note: Probably "voltage" is intended.

forming an island-form polycrystalline layer on the gate insulating film; a step for forming an impurity layer on the surface of the semiconductor layer by implanting impurity ions thereinto; and a step for forming a high-resistance layer and a terminal layer by implanting F ions obliquely into the lower sides of the island-form polycrystalline layer and into the semiconductor layer, respectively.

[0014] In other words, the field-effect transistor of the present invention has the effect of reducing field concentration and impact ionization at the sides of the gate and of reducing the degradation of driving capacity. Factors responsible for this achievement are the presence of a high concentration of the dopant in the lower sides of the gate and the fact that the localized electric field at the sides of the gate is applied on the terminal layer containing a low concentration of defects, and they serve to substantially increase the distance between the gate edge and the operating layer and to reduce the localized-field-induced carriers at the sides of the gate.

[0015]
Description of the Preferred Embodiments:
(First Embodiment) A first embodiment of the present invention will be described next with reference to the accompanying diagrams. However, the same reference numerals are used for the constituent members that are the same as those of the example of the prior art, and detailed explanation thereof will be omitted.

[0016] Fig. 1 is a cross-sectional view of a field-effect transistor having an LDD structure according to the present invention. Whereas the resistance of the conventional gate is uniform, the gate of the present invention has high resistance layers 12, which have a triangular shape when viewed along the cross-sectional axis, at the lower sides of the gate 11 on the gate insulating film 2, as clearly shown by Fig. 1. In other words, the present invention is designed in a manner so that the intensity of the field applied on the two ends of the p-channel formed on the surface of the n-type semiconductor is less than that in conventional transistors.

[0017] Next, the composition and the constitution of each element comprising the field-effect transistor will be described. The gate 11 consists of polycrystalline silicon having a thickness of 3,000 Å and a B concentration of 1×10^{20} cm^{-3} calculated for the implantation of B ions with an acceleration voltage of 30 keV. The high-resistance layer 12 located on both sides of the gate 11 on the side of the gate insulating film 2 is formed by implanting B ions vertically into the gate at a dose of 1×10^{13} cm^{-2} and by implanting F as a dopant obliquely into the gate using a dose of 1×10^{13} cm^{-2}.

[0018] Consequently, the plane impedance of the high-resistance layer 12 is high, 2 kΩ/□, as compared to that of the gate 11 after activation, 50 kΩ/□. Moreover, whereas the capacitance per unit area of the commonly used gate is 4×10^{-5} $pF\mu m^{-2}$, the capacitance at the sides of the gate is reduced to 1×10^{-6} $pF\mu m^{-2}$. As a result, the high-resistance layer 12 suppresses the

generation of field concentration at the sides of the gate, thus providing high resistance to pressure*.

[0019] Moreover, the reduced capacitance due to the high-resistance layer 12 causes a reduction in the parasitic capacitance, thereby increasing the switching speed. Furthermore, the low-concentration layer 8 present below the high-resistance layer 12 with the gate insulating film 2 sandwiched in between is formed by the thermal diffusion of B and contain B at 1×10^{12} cm^{-3} and F at 1×10^{12} cm^{-3}.

[0020] Fig. 2 is a cross-sectional view of the interface of the terminal layer formed on the surface of the n-type semiconductor layer with the gate insulating film. As shown in the diagram, defects in both the terminal layer, which is made of the semiconductor containing the dopant F, and the gate insulating film, which contains F and is an insulator, are eliminated by the F. As described above, because the low-concentration layer contains F, severed bonds, the so-called dangling bonds, which are present in between the gate insulating film and the low-concentration layer, are terminated by F. As a result, the driving capacity of the field-effect transistor is not compromised.

[0021] On the other hand, the source is comprised of a mixed layer formed by implanting F and B ions. In carrying out the ion implantation, the tilt angle, which refers to the angle from the line perpendicular to the base of the gate, is between 15 to 60 degrees. The steps used to manufacture a field-effect transistor according to the first embodiment will be described briefly hereinafter.

[0022] Fig. 3 is a diagram illustrating the steps used to manufacture a field-effect transistor according to the present invention. As shown in Fig. 3a, a gate insulating film 2 with a thickness of 100 to 200Å is first formed on a n-type semiconductor layer 1 composed of monocrystalline silicon by thermal oxidation at a temperature of 850°C to 900°C, and after a polycrystalline layer composed of undoped polycrystalline silicon is deposited on the gate insulating film 2 by CVD, an island-form polycrystalline layer 3 of a 400 nm thickness is formed by patterning the polycrystalline layer, and boron (B) ions are implanted vertically into the n-type semiconductor layer 1 using an acceleration voltage of 10 to 30 keV and a dose of 1×10^{13} to 1×10^{14} cm^{-2}.

[0023] This results in the formation of a p^+ layer 4 having a high B concentration on the surface of the polycrystalline layer 3 lying on the gate insulating film 2 and a p^+ layer 4 on the surface of the n-type semiconductor layer 1 under the gate insulating film 2 to the right and left of the polycrystalline layer, as shown in Fig. 3b. As shown in Fig. 3c, fluorine (F) ions are implanted obliquely as a dopant into the n-type semiconductor layer 1 using an acceleration voltage of 40 keV and a dose of 1×10^{14} cm^{-2}.

---

* Translator's note: Probably "voltage".

[0024] This results in the formation of a high-resistance layer 12 due to the increase in the quantity of dopant (F) on the surface of the gate insulating film 2 to the right and left sides of the polycrystalline layer 3, as shown in Fig. 3d. Moreover, the surface of the n-type semiconductor layer under the gate insulating film is implanted obliquely with F ions to form a terminal layer 13, which lies not only to the right and left of the polycrystalline layer 3 but also extends into the space under the polycrystalline layer to overlap it, by sandwiching the gate insulating film, since these spaces also contain the dopant.

[0025] Next, dangling bonds in the n-type semiconductor layer are terminated by the dopant F by heat treatment carried out at a temperature of 500°C or more. At the same time, B present in the p^+ layer is diffused into the semiconductor layer by thermal diffusion to form a p-layer 5 on the gate insulating film and p-layers 6 under the gate insulating film. A deposition layer 14 is then formed over the entire surface by sputtering using oxidized silicon, as shown in Fig. 3f.

[0026] This is followed by the etching of the deposition layer, which is deposited on the entire surface, in a manner so as to leave intact only the sides of the high-resistance layers 12 on the gate insulating film 2, to form insulative sidewalls 7 on the side of the high-resistance layers 12, as shown in Fig. 3g. After this, BF_2 ions are implanted vertically into the n-type semiconductor layer 1 using an acceleration voltage of 30 to 50 keV and a dose of 1×10^{15} to 1×10^{16} cm^{-2}, as shown in Fig. 3h.

[0027] Because the sidewalls act as a block against BF_2 during implantation, the concentration of impurity (B) in the p layers under the sidewalls is not increased. On the other hand, the implantation causes the layers to the right and left of the side walls to have a high impurity (B) content, thereby making them of low resistance. When heat treatment is then carried out at a temperature of 600°C or more, the field-effect transistor takes on a constitution comprising the following, as shown in Fig. 3i: a gate 11, which has a high impurity concentration; a source 9 having a high impurity concentration; a low-concentration layer 8, in which dangling bonds are terminated by the dopant and which has a low impurity concentration; the n-type terminal layer 13 having a high dopant content; the n-type operating layer; the terminal layer 13; the low-concentration layer 8; and a drain 10 having a high impurity concentration.

[0028] The present embodiment provides a 10% improvement to the pressure* resistance over what is obtained by a uniform gate structure. The following two operations are obtained by a field-effect transistor such as this. In the first place, because the oblique implantation of F ions allows F to be present in the gate insulating film under the two sides of the gate electrode, the generation of B_2O_3 in the gate insulating film is prevented, and this serves to facilitate the penetration of B.

[0029] As a result, the B concentration is reduced only at the right and left of the gate electrode, and this, in turn, serves to decrease the gate-drain overlap capacitance, thereby providing an even faster transistor. Because the parasitic capacitance C is the capacitance of the area where the

---

* Translator's note: Probably "voltage".

gate and source or the gate and drain overlap each other, it stands to reason that it decreases as the insulating distance d increases according to the relational expression $C = \epsilon d/S$ (where: ϵ is the dielectric constant, d the insulation distance, and S the area of overlap).

[0030] According to the relational expression shown below, as the parasitic capacitance decreases, for example, the ring oscillator delay time τ improves.

$\tau = CV/I$ where: C is the ring-oscillator capacitance, V the voltage applied on the ring oscillator, and I the ring-oscillator current.

[0031] In this case, there is a concern that the threshold voltage is changed due to the penetration of B. However, because the B to the right and left of the gate is formed only as an LDD, there is virtually no effect. In the second place, the termination by F of the dangling bonds present in the Si-SiO_2 boundary reduces near-interface states. One of the contributing factors for the degradation of properties of the field-effect transistor is the degradation of the current driving capacity due to the hot carrier phenomenon.

[0032] The hot carrier phenomenon is a phenomenon in which near-interface states are generated in the Si-SiO_2 boundary as a result of the impact ionization of carriers near the drain when hot carriers are injected into the gate insulating film. In the present invention, dangling bonds are terminated by F or Cl to form Si-F (bond energy: 553 kJ/mol) or Si-Cl (bond energy: 358 kJ/mol), respectively. Because the bond energy of these bonds is higher than that of Si-H (bond energy: 299 kJ/mol) or Si-Si (bond energy: 327 kJ/mol), near-interface states are not generated as readily.

[0033] As can be expected from the values given above, F is a more desirable dopant than Cl.

(Second embodiment) Fig. 4 illustrates another sequence of the steps used to manufacture a field-effect transistor according the present invention. However, the same reference numerals are used for the constituent members that are the same as those of the first embodiment, and detailed explanation thereof will be omitted.

[0034] The steps will be described with reference to the accompanying diagrams. As shown in Fig. 4a, an island-form undoped polycrystalline layer 3 is formed on a gate insulating film 2, which, in turn, is formed on a n-type semiconductor layer 1. This is followed by ion implantation in which B ions are implanted vertically into the n-type semiconductor layer 1 under the conditions of 10 keV and 1×10^{13} cm^{-2}. This implantation with the impurity B results in the formation of a p^+ layer on the surface of the polycrystalline layer 3 and p^+ layers on the surface of the n-type semiconductor layer 1, as shown in Fig. 4b.

[0035] As shown in Fig. 4c, a dopant, F, is then ion implanted obliquely into the n-type semiconductor layer 1 under the conditions of 20 keV and 4×10^{13} cm^{-2}. This results in the formation of a high resistance layer 12, which has a high F content and high resistance, at each

of the lower sides of the polycrystalline layer 3, as shown in Fig. 4d. At the same time, a terminal layer 13 is formed under the insulating film 2 to the right and left of the polycrystalline layer, but also extending into the area under it, sandwiching the gate insulating film, since F penetrates into this region as well.

[0036] Next, heat treatment is carried out at 600°C in a deoxygenated environment, to be followed by thermal oxidation at 1,000°C in an oxygen environment. As a result, the impurity and dopant present above and below the gate insulating film are activated by the first heat treatment, and the oxidation of polycrystalline Si progresses with the latter heat treatment, as shown in Fig. 4e. In this manner, a p layer 6 and the terminal layer 13 are formed under the gate insulating film, while a p layer 5, which has become thinner, the high resistance layers 12 and a thermal oxidation film 15 surrounding the previous two are formed on the gate insulating film.

[0037] As shown in Fig. 4f, sidewalls 7 having a thickness of 1,000 nm are then fabricated by etching the thermal oxidation film by removing only the portion on the top surface of the p layer 5. Using the sidewalls thus formed, as shown in Fig. 4g, BF_2 ions are implanted vertically into the n-type semiconductor layer 1 using an acceleration voltage of 40 keV and a dose of 7×10^{15} cm^{-2}.

[0038] This results in a field-effect transistor having a low field concentration at the sides of the gate and a low concentration of near-interface states in the LDD section, as shown in Fig. 4h. The use of the method according to the present embodiment results in the self-aligned formation of the sidewalls.

(Third Embodiment) An undoped polycrystalline layer was used in the aforementioned embodiment, but a layer that is doped during the manufacturing process may also be used over the gate insulating film.

[0039] Fig. 5 is a diagram showing the manufacturing steps for a field-effect transistor using a doped layer. Incidentally, as was the case in the second embodiment, the same reference numerals are used for the constituent members that are the same as those of the first embodiment. As shown in Fig. 5a, a low-resistance semiconductor layer, which is composed of either amorphous silicon (a-Si) containing 1×10^{20} cm^{-3} of an impurity (B) or a polycrystalline Si, is formed on a n-type semiconductor layer 1, on which a gate insulating film 2 has already been formed. Then, an island-form low-resistance semiconductor layer 17 is formed by patterning using a resist 16, and then boron (B) ions are implanted vertically into the n-type semiconductor layer 1 under the conditions of an acceleration voltage of 30 keV and a dose of 1×10^{14} cm^{-2}.

[0040] As shown in Fig. 5b, this results in the formation of a thin p^+ layer 4 on the surface of the n-type semiconductor layer 1, lying under the gate insulating film 2, to the right and left of a p^+ layer covered by the resist 16. As shown in Fig. 5c, the dopant F ions are then implanted

obliquely into the n-type semiconductor layer using an acceleration voltage of 30 keV and a dose of 1×10^{14} cm^{-2}.

[0041] After the dopant is implanted, high-resistance layers 12 are formed at the lower sides of the low-resistance semiconductor layer 17 on the gate insulating film 2, and terminal layers 13 under the gate insulating film, as shown in Fig. 5d. Next, the low-semiconductor layer 17, which is composed of a-Si or polycrystalline Si, is side etched according to the diffusion distance of the next diffusion, as shown in Fig. 5e.

[0042] As shown in Fig. 5f, the resist is then peeled off, and the p layer 6 is formed under the gate insulating film by carrying out thermal diffusion at a temperature of 700°C for one hour. As shown in Fig. 5g, BF_2 ions are implanted vertically into the entire surface of the n-type semiconductor layer 1 under the conditions of an acceleration voltage of 50 keV and a dose of 1×10^{16} cm^{-2}. This results in a field-effect transistor having the following the constitution: gate 11 with a high-resistance layer 12, which has a high F content and located at its lower sides, on the gate insulating film 2; and, under the gate insulating film, a p^+-type source 9, the n-type terminal layer 13, an n-type operating layer, the n-type terminal layer 13 and a p^+-type drain 10.

[0043] According to the present embodiment, ion implantation has to be carried out on the gate only once. Although the present embodiment dealt with a field-effect transistor formed on an n-type semiconductor layer, the substrate used for the n-type semiconductor should not be limited to semiconductor wafers, but insulating substrates such as quartz substrates or sapphire substrates may also be used.

[0044] With the field-effect transistor of the present invention, the lower sides of the gate have high resistance. Because of this, only slight field concentration takes place there, and this serves to reduce the fluctuations in the drain current with respect to the gate voltage over time, thus extending the lifetime of the driving capacity. Moreover, because its high resistance section is long along the cross-sectional axis of the gate section, but short on the surface side of the gate, the gate resistance can be reduced as compared with one which is built to have simply the same length along the depth of the gate.

[0045]
Operation: The field-effect transistor of the present invention provides reduced field concentration at the sides of the gate and high resistance against pressure*.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a cross-sectional view of a field-effect transistor having a nonuniform gate according to the present invention.

---

* Translator's note: Probably "voltage".

Fig. 2 is a diagram illustrating the actions of the phenomenon of termination by F according to the present invention.

Fig. 3 is an illustration of the manufacturing steps for a field-effect transistor having a nonuniform gate with deposition walls according to the present invention.

Fig. 4 is an illustration of the manufacturing steps for a field-effect transistor having a nonuniform gate with oxidation walls according to the present invention.

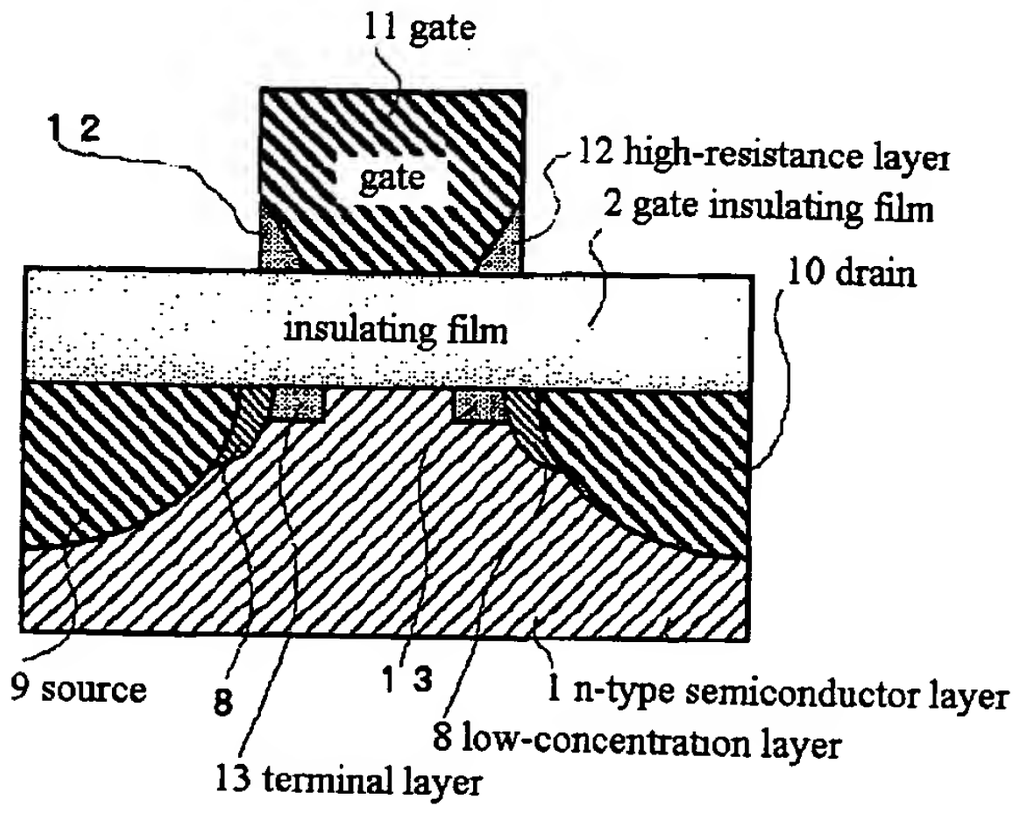
Fig. 5 is an illustration of the manufacturing steps for a field-effect transistor having an initially doped nonuniform gate according to the present invention.

Fig. 6 is an illustration of the manufacturing steps for the conventional field-effect transistor having a uniform gate.

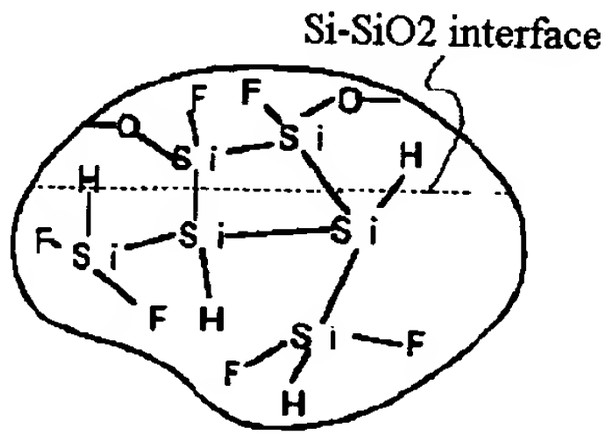
Description of the Reference Numerals

1 n-type semiconductor layer
2 gate insulating film
3 polycrystalline layer
4 p^+ layer
5 p layer
6 p layer
7 sidewall
8 low-concentration layer
9 source
10 drain
11 gate
12 high-resistance layer
13 terminal layer
14 deposition layer
15 thermal oxidation layer
16 resist
17 low-resistance semiconductor layer

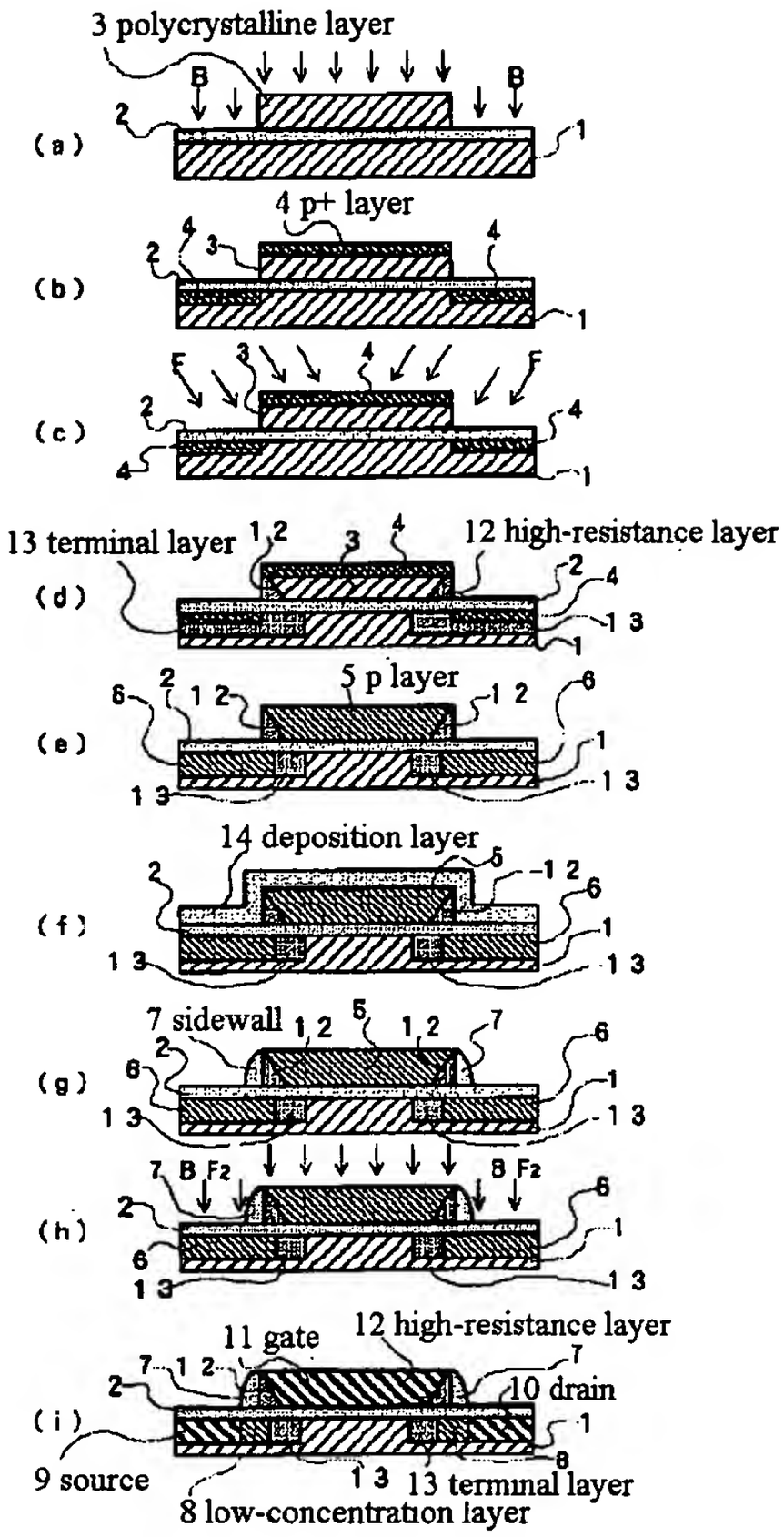
【図１】



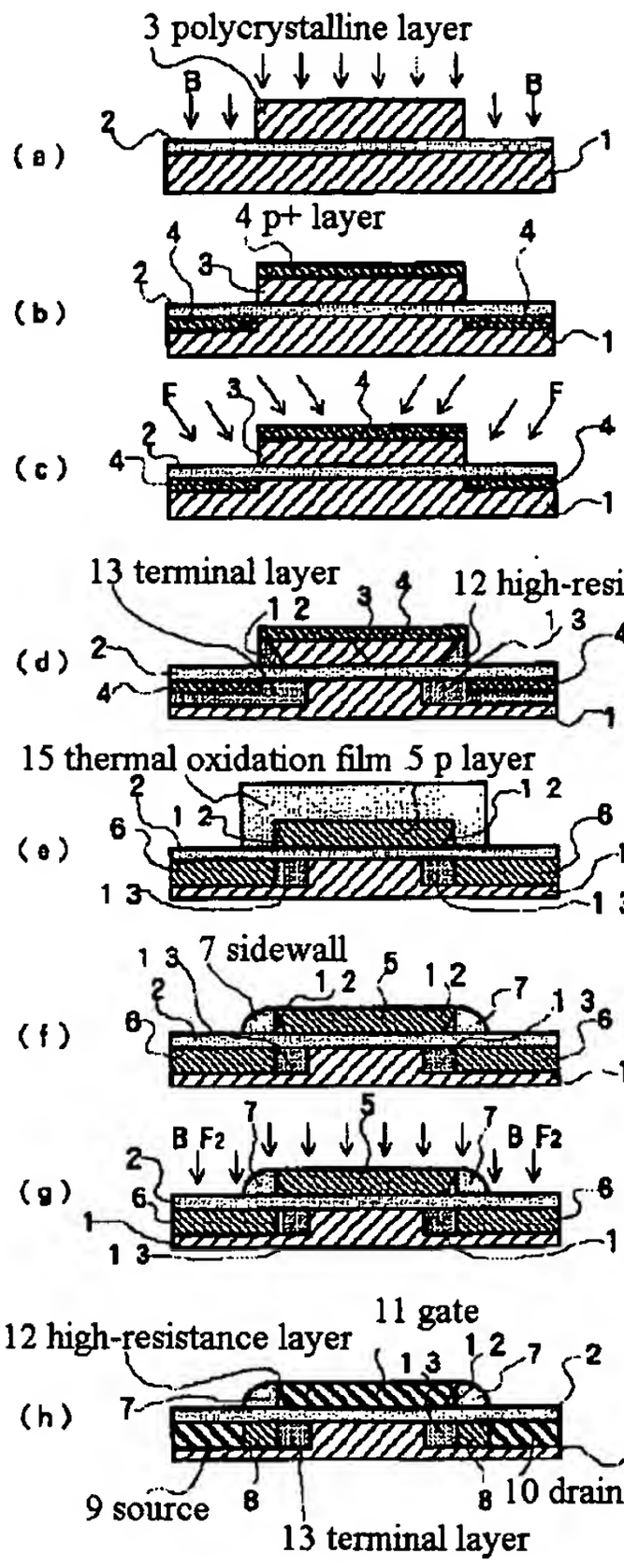
【図２】



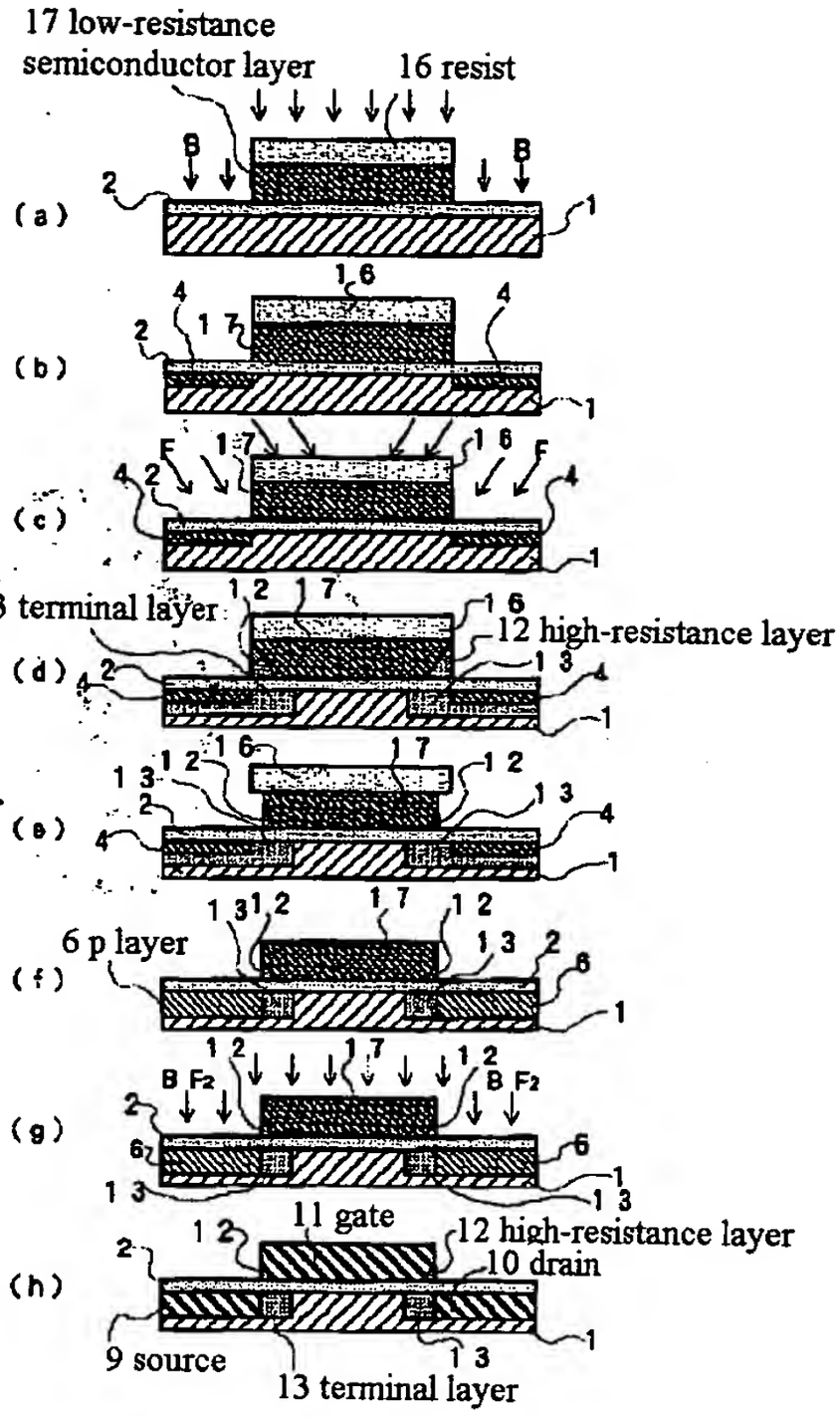
【図３】


3 polycrystalline layer
B
B
2
1
(a)
4 p+ layer
4
3
4
2
1
(b)
F
3
4
F
2
4
4
1
(c)
13 terminal layer
1,2
3
4
12 high-resistance layer
2
4
1 3
1
(d)
5 p layer
6
2
1 2
1 2
6
1
1 3
1 3
(e)
14 deposition layer
2
5
1 2
6
1
1 3
1 3
(f)
7 sidewall
1 2
5
1 2
7
2
6
6
1
1 3
1 3
(g)
7
B F2
B F2
2
6
6
1
1 3
1 3
(h)
11 gate
12 high-resistance layer
7
7
1 2
10 drain
2
1
(i)
9 source
1 3
13 terminal layer
8
8 low-concentration layer

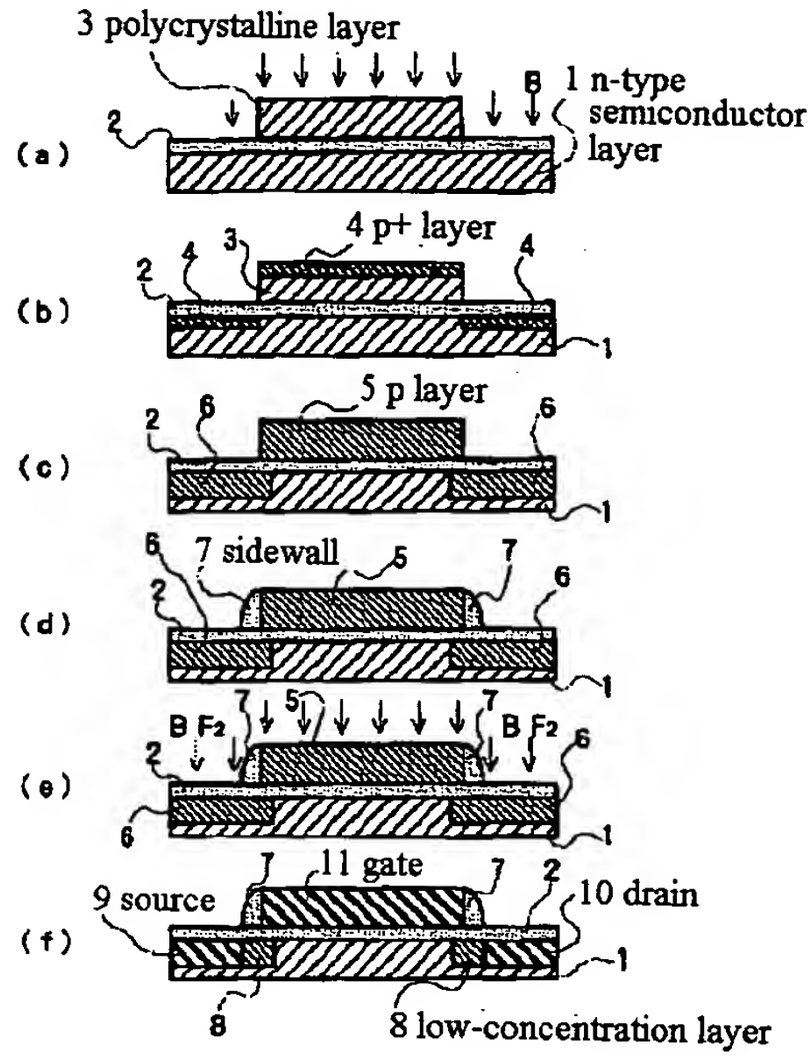
【図４】


3 polycrystalline layer
B
B
2
1
(a)
4 p+ layer
4
3
4
2
1
(b)
F
3
4
F
2
4
4
1
(c)
13 terminal layer
1 2
3
4
12 high-resistance layer
1 3
2
4
4
1
(d)
15 thermal oxidation film 5 p layer
2
1 2
1 2
6
6
1
1 3
1 3
(e)
1 3
7 sidewall
1 2
5
1 2
7
1 3
2
6
6
1
(f)
7
5
7
B F2
B F2
2
6
6
1
1 3
1 3
(g)
11 gate
12 high-resistance layer
1 3
1 2
7
2
7
1
(h)
9 source
8
8
10 drain
13 terminal layer

【図５】


17 low-resistance semiconductor layer
16 resist
B
B
2
1
(a)
1 6
4
1 7
4
2
1
(b)
F
1 7
1 6
F
4
2
4
1
(c)
3 terminal layer
1 2
1 7
1 6
12 high-resistance layer
1 3
4
2
4
1
(d)
1 6
1 7
1 2
1 2
1 3
1 3
2
4
4
1
(e)
6 p layer
1 3
1 2
1 7
1 2
1 3
2
6
1
(f)
B F2
B F2
1 2
1 7
1 2
2
6
6
1
1 3
1 3
(g)
11 gate
12 high-resistance layer
1 2
10 drain
2
(h)
9 source
1 3
13 terminal layer
1

【図６】


3 polycrystalline layer
B
B
1 n-type semiconductor layer
2
(a)
4 p+ layer
3
2
4
4
(b)
5 p layer
2
6
6
1
(c)
7 sidewall
5
6
7
2
6
1
(d)
B F2
B F2
7
5
7
2
6
6
1
(e)
11 gate
9 source
10 drain
7
2
1
(f)
8
8 low-concentration layer